Tentative Schedule

25/07/2016 Day 1 (MONDAY)		
10:00 –11:30 AM	Prof. Mohammad Hasan	Introduction to VLSI and Digital System Design
03:00 - 04:30 PM	Prof. Mohammad Hasan	FPGA based system design
26/07/2016 Day 2 (TUESDAY)		
10:00 –11:30 AM	Prof. Mohammad Hasan	Low power architectures for DSP algorithms
03:00 - 04:30 PM	Mohammad Wajid	Lab session (provisory): Logic implementation on FPGA using Xilinx ISE
27/07/2016 Day 2 (WEDNESDAY)		
03:00 - 04:30 PM	Prof. B. K Mohanty	Design-space exploration of hardware accelerators
28/07/2016 Day 3 (THURSDAY)		
10:00 –11:30 AM	Prof. B. K Mohanty	Design-space exploration of hardware accelerators
03:00 - 04:30 PM	Prof. B. K Mohanty	Design-space exploration of hardware accelerators
29/07/2016 Day 4 (FRIDAY)		
10:00 –11:30 AM	Dr. Ashwani Rana	Low power design techniques
03:00 - 04:30 PM	Dr. Shubhajit Roy Chowdhury	Architectural Design of Integrated Circuits
30/07/2016 Day 5 (SATURDAY)		
10:00 –11:30 AM	Dr. Rajesh Kumar	Spintronics: advances, approaches and applications
03:00 - 04:30 PM	Prof. Arun Kumar	Advances in human and machine speech communication-I
31/07/2016 Day 6 (SUNDAY)		
10:00 –11:30 AM	Prof. Arun Kumar	Advances in human and machine speech communication-II

Objective

The objective of this short term course is to enhance the theoretical and practical knowledge of the faculty and research scholars in VLSI, Signal Processing, and VLSI for Signal Processing to explore the open research arena in these areas.

The signal processing algorithms are computationally intensive and are real time in nature. These algorithms are required to be mapped into application specific architectures for the implementation using ASIC and FPGA, which we shall be covering through this course.

Patrons

Prof. S. C. Saxena,
Vice-Chancellor, JUIT, Waknaghat

Brig. K. K. Marwah (Retd.),
Registrar

Prof. Samir DevGupta,
Director & Academic Head

Program Chair

Prof. Sunil Bhooshan
HoD, ECE

Program Convenor

Mohammad Wajid
Assistant Professor, Dept. of ECE

Program Co-ordinators

Dr. Meenakshi Sood & Dr. S D Sharma
Assistant Professors, Dept. of ECE

Contact:

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This event has been supported by IEEE SB JUIT

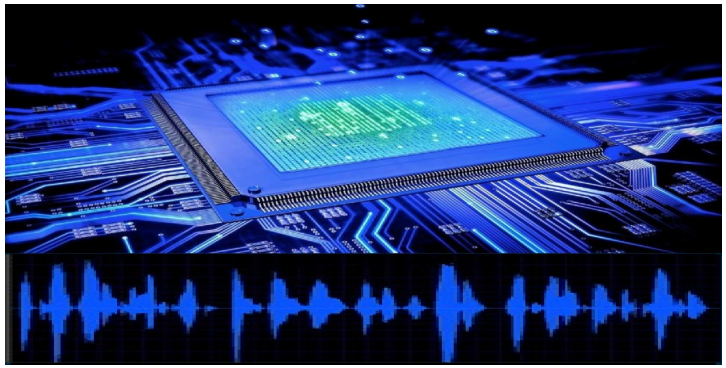
SHORT TERM COURSE ON

Advances in VLSI and Signal Processing

25 –31 July 2016

Organized by:

Dept. of Electronics & Communication Engineering
Jaypee University of Information Technology, Solan



Registration

Registration fee - INR 1500/-
Last date for registration– 15 July, 2016

Participants can register by sending the duly filled registration form along with the Demand Draft (in favor of "Jaypee University of Information Technology" payable at Shimla) of Rs. 1500/- to the following address by the registered post.

Mohammad Wajid, Department of ECE,
Jaypee University of Information Technology
Waknaghat, Solan, Himachal Pradesh-173234

Link for paid accommodation

Resource Persons

Prof. Arun Kumar

C.A.R.E., IIT Delhi

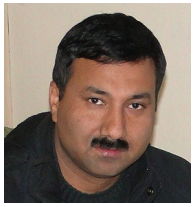
Prof. Arun Kumar did his B.Tech, M.Tech and PhD, in Electrical Engineering, from the Indian Institute of Technology, Kanpur. He was a Visiting Researcher at the University of California, Santa Barbara, from 1994 to 1996, prior to joining the Indian Institute of Technology, Delhi in 1997. He is a recipient of the Young Scientist Award of the International Union of Radio Science (URSI)

Prof. B.K Mohanty

ECE Dept., JUET

Prof. Mohanty received his Ph.D degree in VLSI for Digital Signal Processing from Berhampur University. His research interest includes algorithm design, mapping and implementation for high-performance, resource-constrained multimedia signal processing applications and secured communication. He also serves as the reviewers of IEEE Transactions , IET and Springer journals related to VLSI for Signal Processing.

Dr. Ashwani Rana



ECE Dept., NIT Hamirpur

Dr. Ashwani K. Rana received his B.Tech degree in Electronics and Communication Engineering from National Institute of Technology, Hamirpur, India and M.Tech degree in VLSI Technology from Indian Institute of Technology, Roorkee, India. He did his Ph.D degree from National Institute of Technology, Hamirpur. His research interest includes low power high performance VLSI circuit design, emerging integrated circuit technologies and modeling of semiconductor devices.

Resource Persons

Prof. Mohammad Hasan

Electronics Engg. Dept., AMU

Prof. Hasan completed his PhD from the University of Edinburgh, UK on a Commonwealth Scholarship in "Low Power Architectures for Signal Processing and Communications". He also worked as a Visiting Researcher in Royal Academy of Engineering, UK funded project on "Low Power FPGA". He has filed three patents on the design of magnetic RAM (MRAM) and one patent on robust SRAM.

Dr. Shubhajit Roy Chowdhury

School of CEE, IIT Mandi

Dr. Shubhajit Roy Chowdhury did his M.Tech and PhD from the Jadavpur University. He was gold medalist in M.Tech as well as B.Tech programme. His research interest includes VLSI Architectures, Biomedical Embedded Systems, Non invasive diagnostic systems, etc. Prior to joining IIT mandi, he was associated with IIIT Hyderabad, Indian Statistical Institute, Kolkata, and Jadavpur University.

Dr. Rajesh Kumar

JUIT, Waknaghat

Rajesh Kumar obtained his M.Tech. from IIT Roorkee and Ph.D. in Physics (Nanotechnology) from H.P. University, Shimla. He has worked as a researcher in the Center for Superfunctional Materials (CSM) at Pohang University of Science and Technology (POSTECH), South Korea. He is also a Visiting Professor at GIST, South Korea. He is a visiting scientist in Kyushu University, Japan (on a DST-JSPS sponsored collaborative project).

IEEE
Student Branch JUIT

Registration Form

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SHORT TERM COURSE

On

Advances in VLSI and Signal Processing

25 –31 July, 2016

Last date for registration: 15 July, 2016

Name: _____

Designation: _____

Qualification: _____

Institution: _____

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Mobile: _____

Email: _____

Demand Draft Details:

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Signature of participant

Also send the scanned copy of this registration form, Identity card, and demand draft to email address:

meenakshisood@juit.ac.in *or*
mohd.wajid@juit.ac.in