# Two Days VLSI (Cadence Design Tools) Workshop on June 05-06, 2023

## Electronics and Communication Engineering Department

## Jaypee University of Information Technology, Waknaghat, Himachal Pradesh

Electronics and Communication Engineering Department, JUIT, organized a "Two Days VLSI (Cadence Virtuouso) Workshop on June 05-06, 2023" in Physical (Hands On Practice) as well as Online Mode (https://meet.google.com/qss-qjwq-pni) . The two day training program was a part of the the license which ECE department, JUIT bought the license from Entuple Technologies Pvt. Ltd. in February, 2023. In consists of 10 licenses. In line with the Government of India VLSI initiative, JUIT has gone ahead in providing the Faculty and students with state art VLSI tools (Cadence Design Tools: Analog, Digital).

The Onsite training workshop was conducted and training was provided on '**Cadence Design Flow: Analog and Digital Circuit Design**' in Mitsubishi Factory Automation Lab (ECL6), Vivekanand Bhawan (Academic Block), JUIT Waknaghat. The training was conducted by Mr. Anish Kumar from 5$^{th}$ June to 6$^{th}$ June 2023 and was focused on **Analog Design** using **Cadence Custom IC Design Tools** following with Schematic capture, Analog Simulations, Layout Extraction, Physical verification and Post Layout Simulation and **Digital Design** using **Cadence ASIC Design Tools** following with RTL Design, functional simulations, synthesis, and Physical design. The training went well and participants shall practice the tools later and if any problem is faced then we can always contact the expert person of Entuple Technologies Pvt. Ltd. for further help.

**Resource Person**: Mr. Anish.K.Sharma,

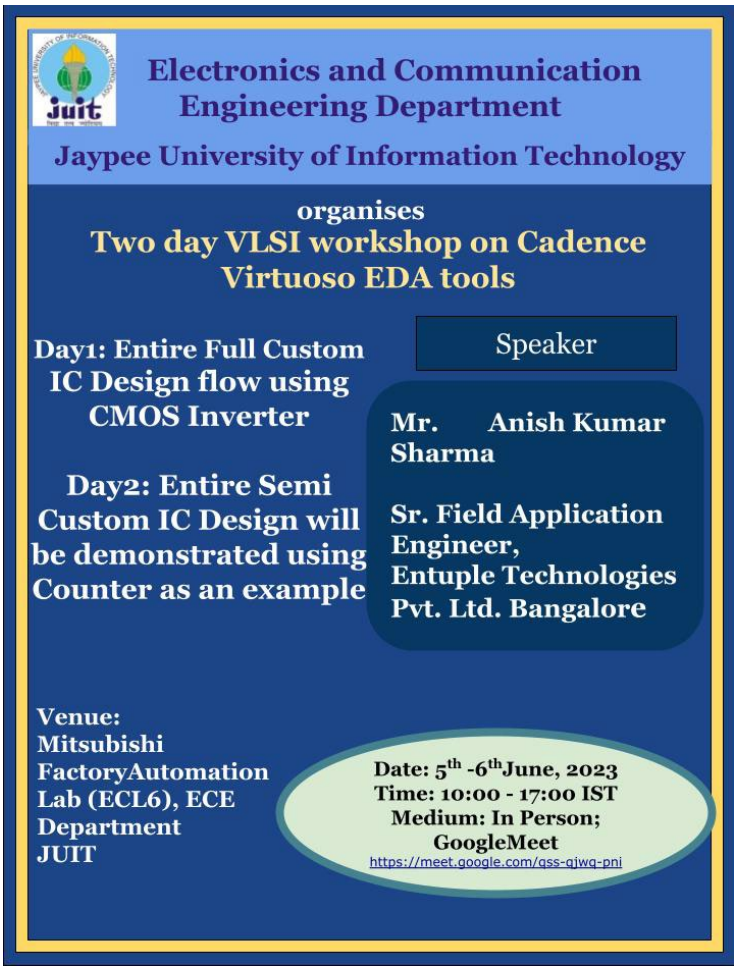
Sr. FAE, Entuple Technologies Pvt. Ltd.

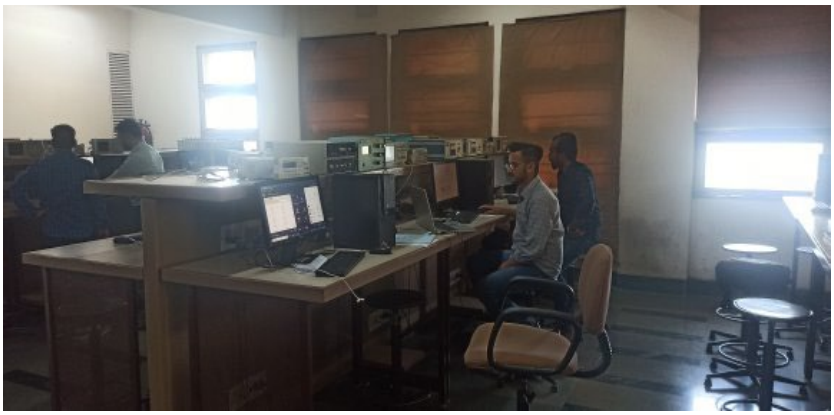
**Venue**: Mitsubishi Factory Automation Lab (ECL6)

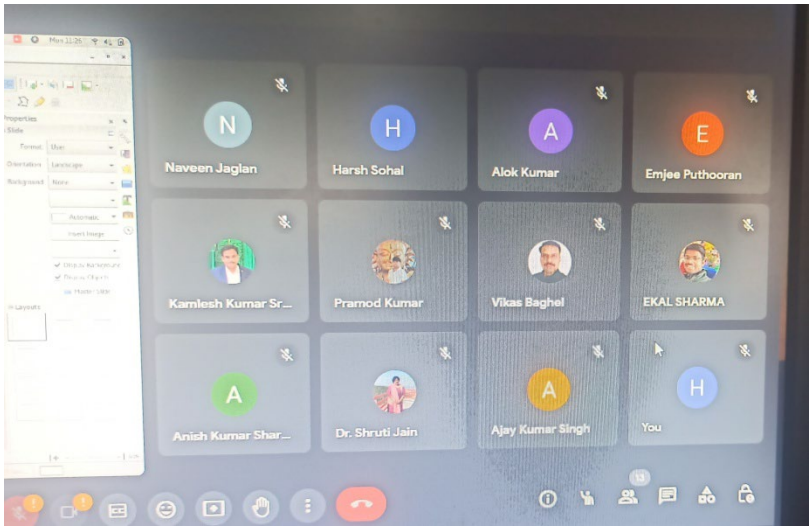
Vivekanand Bhawan (Academic Block), JUIT Waknaghat

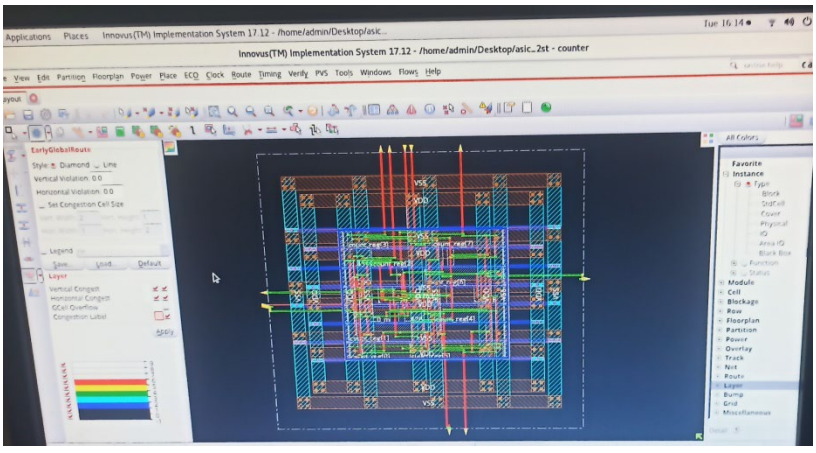
**Online Link**: https://meet.google.com/qss-qjwq-pni

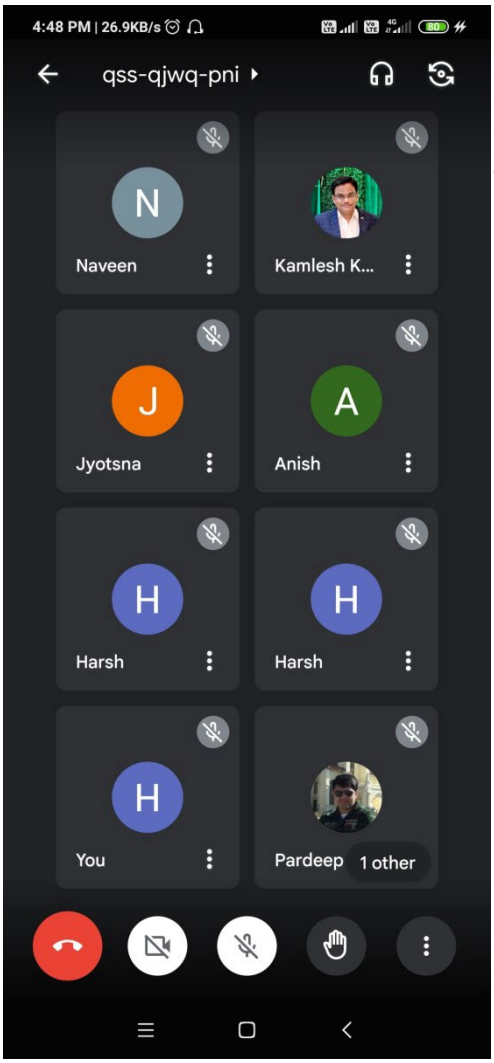
**Co-ordinated by**: Dr. Harsh Sohal, Associate Professor, ECE Department, JUIT

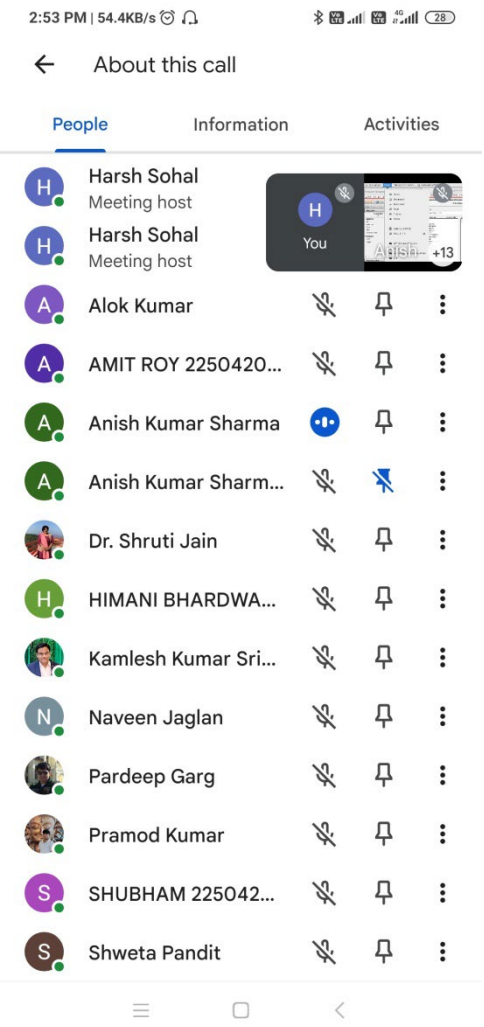

Electronics and Communication Engineering Department
Jaypee University of Information Technology
organises
Two day VLSI workshop on Cadence Virtuoso EDA tools
Day1: Entire Full Custom IC Design flow using CMOS Inverter
Day2: Entire Semi Custom IC Design will be demonstrated using Counter as an example
Speaker
Mr. Anish Kumar Sharma
Sr. Field Application Engineer, Entuple Technologies Pvt. Ltd. Bangalore
Venue: Mitsubishi FactoryAutomation Lab (ECL6), ECE Department JUIT
Date: 5th -6thJune, 2023
Time: 10:00 - 17:00 IST
Medium: In Person; GoogleMeet
https://meet.google.com/qss-qjwq-pni




Naveen Jaglan
Harsh Sohal
Alok Kumar
Emjee Puthooran
Kamlesh Kumar Sr...
Pramod Kumar
Vikas Baghel
EKAL SHARMA
Anish Kumar Shar...
Dr. Shruti Jain
Ajay Kumar Singh
You


Innovus(TM) Implementation System 17.12 - /home/admin/Desktop/asic_2st - counter




## The Workshop Schedule:

### Day-1: *Session-1: (10 am - 1 pm)*

- Introduction to Full Custom IC Design Flow
- Cadence Solutions for Custom IC Design
- Schematic Capture using Virtuoso Schematic Editor
- Symbol Creation
- Testbench Creation using Virtuoso Schematic Editor

 Functional Simulation using Spectre

***Session-2: (2 pm - 5 pm)***

 Layout Design using Virtuoso Layout Editor

 Physical Verification which includes DRC & LVS

 Parasitic Extraction using Quantus

 Post Layout Simulation

 Generation of GDSII

**Note**: By considering, CMOS INVERTER as an example will demonstrate thee ntire Full Custom IC Design Flow

## Day-2: *Session-3: (10 am - 01 pm)*

 Introduction to Semi-Custom IC Design Flow

 Cadence Solutions for Semi-Custom IC Design

 Functional Verification using Incisive

 RTL Synthesis using Genus Synthesis Solution

***Session-4: (2 pm - 5 pm)***

 Physical Implementation using Innovus that includes

Floor Planning; Power Planning; Placement; CTS; Routing

 Timing Analysis

 Power Analysis

 Parasitic Extraction

 Generation of GDSII

**Note**: By considering COUNTER as an example will demonstrate the entire

Semi-Custom IC Design Flow

## List of Attendees:

| **Two Days VLSI (Cadence Tools) Workshop on June 05-06, 2023** | | |
|---|---|---|
| **Electronics and Communication Engineering Department** | | |
| **Jaypee University of Information Technology** | | |
| | | |
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**Prepared by:**

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